

A METHOD TO IMPROVE THE EFFICIENCY OF SYNCHRONOUS MIRROR DELAYS

ABSTRACT

5 A phase detection system for use with a synchronous mirror delay or a delay-locked loop in
order to reduce the number of delay stages required, and therefore increase the efficiency, is
disclosed. The invention includes taking a clock input signal and a clock delay or feedback signal,
each having timing characteristics, and differentiating between four conditions based upon the
timing characteristics of the signals. The phase detector and associated circuitry then determines,
10 based upon the timing characteristics of the signals, which of a number of phase conditions the
signals are in. Selectors select the signals to be introduced into the synchronous mirror delay or
delay-locked loop by the timing characteristics of the phase conditions. The system is able to utilize
the falling clock edge of the clock input signal, and the lock time is decreased under specific phase
conditions. The invention increases the efficiency of the circuits by reducing the effective delay
stages in the SMD or DLL while maintaining the operating range.